Research Article

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Design and Analysis of Approximate 4:2 Compressors for High Performance Multiplier

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Abstract

The quest for high-speed computing with optimal power usage has spurred the rise of approximate computing, a methodology that sacrifices precision for improved power efficiency. This paper delves into the realm of approximate computing by exploring the power consumption aspects of both existing and novel architectures of approximate 4:2 compressors. Employing Intel Quartus Prime, the study seeks to elevate the performance metrics of multipliers. By scrutinizing the power consumption characteristics, the research aims to shed light on the efficacy of approximate computing in real-world scenarios. Through meticulous analysis, it intends to uncover the trade-offs between accuracy and energy consumption, elucidating the potential benefits and drawbacks of adopting approximate computing methodologies in practical applications. The investigation into 4:2 compressors serve as a microcosm for broader discussions surrounding approximate computing's role in contemporary computing paradigms. It endeavors to provide insights into how approximate computing techniques can be harnessed to bolster the efficiency and performance of computational systems, particularly in scenarios where stringent power constraints coexist with the demand for high computational throughput.

Keywords: VLSI, Compressors, Approximate Compressor, Approximate Computing, Inexact Computing, Multiplier, Approximate Multiplier, Low Power Design, Power Analysis

1. Introduction

Over the past two decades, the semiconductor industry has witnessed remarkable advancements focused on optimizing intricate multimedia applications. The primary objective has been to streamline operations and elevate the portability of electronic devices. During this period, extensive efforts have been dedicated to addressing pivotal hurdles within the realm of Very Large-Scale Integration (VLSI). Innovations in semiconductor technology have paved the way for transformative changes in how multimedia applications are managed and processed. The complexity inherent in multimedia tasks, such as video streaming, image processing, and augmented reality, necessitated the development of more efficient and streamlined solutions. Consequently, researchers and engineers have been fervently engaged in endeavors aimed at enhancing the performance and versatility of electronic devices.

Within the VLSI domain, considerable attention has been directed towards overcoming various challenges associated with integrating numerous components onto a single chip. This pursuit has been driven by the increasing demand for compact yet powerful electronic devices capable of handling diverse multimedia tasks seamlessly. Researchers have focused on optimizing chip design, exploring novel architectures, and refining manufacturing processes to achieve higher levels of integration and efficiency. One of the key areas of innovation has been in the development of specialized hardware accelerators tailored for multimedia applications. These accelerators are designed to offload specific tasks from the main processor, thereby improving overall system performance and power efficiency. By leveraging dedicated hardware for tasks such as video encoding, image recognition, and audio processing, electronic devices can deliver enhanced user experiences while conserving energy.

Furthermore, advancements in semiconductor manufacturing technologies have played a pivotal role in driving progress within the VLSI domain. Shrinking transistor sizes, improving lithography techniques, and enhancing material properties have enabled the fabrication of increasingly complex and energy-

efficient chips. This has not only facilitated the integration of more functionality onto single chips but has also contributed to reducing production costs and enhancing scalability. The relentless pursuit of innovation within the semiconductor industry has resulted in a proliferation of multimedia-enabled electronic devices that have become indispensable in modern society. From smartphones and tablets to smart TVs and wearable gadgets, these devices owe their performance and portability to the continuous advancements in VLSI technology. Looking ahead, further breakthroughs in semiconductor research and development are poised to revolutionize the landscape of multimedia applications, ushering in new possibilities for connectivity, entertainment, and productivity.

The imperative to minimize area, power consumption, and enhance application speed has been a driving force behind the development of integrated circuits. However, specific applications like image processing and multimedia demand optimization in power consumption, leading to the emergence of approximate computing as a viable solution. Approximate computing has recently emerged as a promising approach to enhance circuit performance by relaxing the demand for exact calculations. This involves trading computation accuracy for reduced computational efforts, offering a pragmatic design methodology. The overhead incurred by computation units in processors to achieve high performance and execution efficiency often results in significant power consumption. Approximate computing presents an opportunity to address this issue, as approximation in arithmetic operations leads to faster systems with reduced design complexity and power consumption. Present research endeavors are primarily focused on delving into approximate 4:2 compressors, with the explicit goal of augmenting the efficacy of multipliers while concurrently mitigating power usage. This pursuit necessitates thorough scrutiny and evaluation of antecedent high-performance 4:2 compressors to discern methodologies conducive to the realization of top-tier multipliers.

The core objective lies in refining the design and operational efficiency of multipliers, a critical component in various computational systems. By delving into the intricacies of 4:2 compressors, researchers aim to devise methodologies that not only bolster the performance metrics of multipliers but also curtail their energy consumption, thus aligning with the contemporary emphasis on sustainability and energy efficiency in semiconductor technologies. The investigative process entails a meticulous examination of prior high-performance 4:2 compressors, scrutinizing their architectural attributes, operational mechanisms, and efficacy in diverse computational scenarios. This comprehensive analysis serves as the foundation for identifying and elucidating strategies pivotal to the development of high-performance multipliers.

Central to this pursuit is the concept of approximation, wherein a trade-off between precision and computational overhead is carefully calibrated to optimize performance while minimizing energy consumption. By harnessing approximate 4:2 compressors, researchers endeavor to strike an optimal balance that maximizes computational efficiency without compromising accuracy to an unacceptable degree. Furthermore, the integration of advanced analytical tools and simulation techniques facilitates a nuanced understanding of the intricate dynamics governing the operation of 4:2 compressors and their impact on multiplier performance. Through rigorous experimentation and validation, researchers aim to validate the efficacy of proposed methodologies and iteratively refine them to achieve superior performance outcomes. The implications of this research extend beyond the realm of theoretical inquiry, as the development of high-performance multipliers holds significant practical relevance in a myriad of applications spanning from signal processing and digital communication to artificial intelligence and scientific computing. By enhancing the efficiency of multipliers, researchers endeavor to unlock new avenues for innovation and advancement across diverse domains reliant on computational prowess.

In essence, the ongoing exploration of approximate 4:2 compressors epitomize a concerted effort to push the boundaries of multiplier performance while adhering to the imperative of energy efficiency. Through meticulous analysis, strategic refinement, and empirical validation, researchers strive to chart a course towards the realization of next-generation multipliers that transcend conventional benchmarks and pave the way for transformative advancements in semiconductor technology. Approaches for dealing with inaccurate partial products in multipliers commonly involve logic simplification techniques such as Karnaugh maps (K-maps) or other methods to streamline the generation logic of products, thereby reducing circuit complexity. These strategies play a crucial role in optimizing the performance of multipliers and contribute to overall advancements in the VLSI domain.

In summary, the ongoing research in approximate 4:2 compressors represent a significant step towards enhancing the efficiency and performance of multipliers, thereby contributing to the continued evolution of integrated circuits and addressing the demands of modern electronic devices.

2. Literature Survey

In the study conducted by T. Kong and S. Li, titled "Design and Analysis of Approximate 4–2 Compressors for High-Accuracy Multipliers," published in IEEE Transactions on Very Large-Scale Integration (VLSI) Systems, Volume 29, Issue 10, pages 1771-1781, the authors explore the design and analysis of approximate 4:2 compressors for high-accuracy multipliers. Their work focuses on developing compressors that can effectively balance accuracy and performance in multiplier designs. By employing novel techniques and methodologies, Kong and Li propose innovative solutions to address the challenges associated with power consumption and computational accuracy in multiplier circuits.

Additionally, P. J. Edavoor, S. Raveendran, and A. Rahulkar presented a study titled "Approximate Multiplier Design Using Novel Dual-Stage 4:2 Compressors," published in IEEE Access.

Their research introduces a novel approach to approximate multiplier design utilizing dual-stage 4:2 compressors. Through comprehensive simulations and analyses, Edavoor et al. demonstrate the effectiveness of their proposed methodology in achieving significant improvements in performance and efficiency compared to conventional multiplier designs. Their work contributes valuable insights into the development of efficient approximate multiplier architectures.

By incorporating findings from these studies, the present research aims to build upon existing knowledge and methodologies to further enhance the design and performance of approximate 4:2 compressors for multipliers, thereby contributing to advancements in the field of VLSI design and optimization.

In summary, the literature survey highlights the significance of approximate computing techniques and the contributions of recent studies by Kong and Li, as well as Edavoor et al., in advancing the design and analysis of approximate multiplier architectures.

3. Approximate Multipliers

In this research endeavor, we present a pioneering approach to the design of a 4-2 compressor, seamlessly integrating it with approximate multiplication methodologies. Our objective revolves around optimizing the critical path within the circuit by harnessing the inherent characteristics of the compressor's truth table.

Moreover, we advance sorting techniques through the utilization of reverse logic gates in constructing a highly accurate 4:2 compressor. This advancement contributes significantly to the evolution of high-performance multipliers [1].

A multiplier stands as a cornerstone in facilitating efficient computations, exerting profound impacts across diverse domains such as image processing and Artificial Intelligence (AI). Its lifecycle encompasses critical stages including partial product generation, depletion, and carry propagation, each pivotal in computing accurate results. To alleviate the overheads associated with partial product computation, multi-operand adders emerge as indispensable components, with compressors emerging as standout structures among them. Multipliers find extensive application in fields like image processing and Artificial Intelligence (AI), where achieving a delicate balance between precision and performance is imperative. Herein lies the importance of employing approximate compressors. Enhancements in any single parameter - whether it be speed, size, or power consumption - invariably bolster the overall performance metrics of the multiplier.

Our research delves into the intricacies of compressor design, recognizing its pivotal role in shaping the efficiency and effectiveness of multipliers. By integrating novel methodologies with established principles, we aim to push the boundaries of performance, laying the groundwork for enhanced computational capabilities across various applications. The integration of approximate multiplication techniques with the innovative design of the 4-2 compressor represents a significant leap forward in the realm of computational efficiency. Through meticulous experimentation and analysis, we demonstrate the efficacy of our approach in mitigating critical path delays and enhancing overall multiplier performance. Furthermore, our utilization of reverse logic gates in crafting a highly precise 4:2 compressor underscores our commitment to advancing the state-of-the-art in multiplier design. By leveraging unconventional techniques, we unlock new avenues for optimizing circuitry and maximizing computational throughput.

In conclusion, our research underscores the indispensable role of compressors in multiplier design and highlights the transformative potential of approximate multiplication methodologies. By pushing the boundaries of conventional design paradigms, we pave the way for more efficient and powerful computational systems, poised to drive innovation across a myriad of domains.

4. Approximate 4:2 Compressors

A 4:2 compressor is a crucial component in digital circuit design, especially in applications where data needs to be efficiently compressed for further processing. This type of compressor takes four inputs and produces two outputs, effectively reducing the number of bits required to represent the data while preserving essential information. Its significance lies in its ability to minimize circuit complexity and speed up operations, making it indispensable in modern digital systems.

The primary function of a 4:2 compressor is to identify and compress patterns within the input data. It achieves this by examining the input bits and determining common characteristics that can be represented with fewer output bits. By identifying redundancies or patterns in the input, the compressor can efficiently reduce the amount of data that needs to be processed or transmitted.

One common implementation of a 4:2 compressor involves the use of parallel comparison and selection circuits. These circuits compare groups of input bits and select the most significant bits to represent the data. Through careful design and optimization, this approach can achieve high levels of compression while maintaining accuracy and speed.

At the heart of a 4:2 compressor are XOR gates, AND gates, and multiplexers, which work together to perform the compression operation. XOR gates are used to detect differences between input bits, while AND gates are employed to identify common patterns. Multiplexers then select the appropriate output bits based on the comparison results, effectively reducing the number of bits required to represent the data.

The design of a 4:2 compressor involves careful consideration of factors such as speed, area, and power consumption. Engineers must balance these competing requirements to create an efficient and reliable compressor that meets the needs of the target application. Techniques such as pipelining, parallelism, and optimization

algorithms are often employed to maximize performance while minimizing resource usage.

In addition to traditional binary inputs, 4:2 compressors can also be designed to handle other data formats, such as Gray code or ternary logic. This flexibility allows them to be used in a wide range of applications, from arithmetic operations in microprocessors to data compression in communication systems.

Overall, the 4:2 compressor plays a vital role in digital circuit design by efficiently compressing data while preserving essential information. Its ability to reduce the number of bits required to represent data makes it an invaluable tool for optimizing performance and reducing resource usage in modern digital systems. By carefully designing and implementing 4:2 compressors, engineers can create more efficient and reliable digital circuits for a variety of applications.

5. Existing Approximate 4:2 Compressors

5.1. Existing Approximate 4:2 Compressor (Architecture 1)

The existing architecture 1 for 4:2 approximate compressor is shown in Figure1.

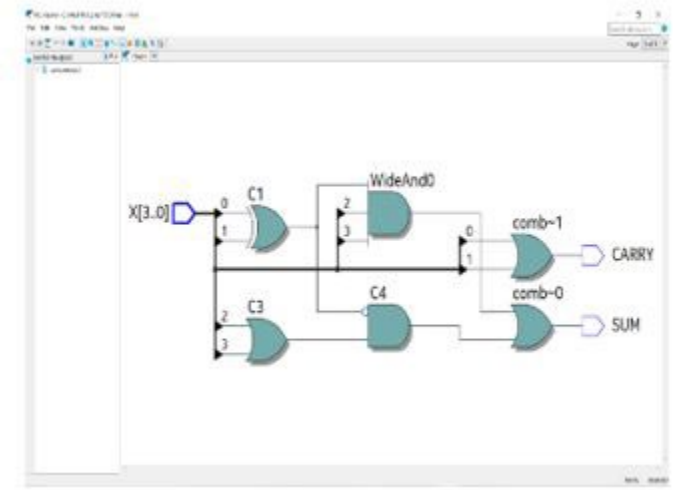

Figure1: Schematic Diagram of Existing Approximate 4:2 Compressor (Architecture 1)

The compressor has four inputs designated as A1, A2, A3, and A4, with corresponding outputs labeled CARRY and SUM. The logical expressions defining the SUM and CARRY outputs are presented below.

SUM= (A1⊕A2)A3A4 + (A1⊕A2)(A3 + A4)

CARRY= A1+A2

Upon examination of the truth table (Table 1) for the current 4:2 compressor architecture, it has been noted that erroneous outputs occur for specific input configurations, namely (0011), (0100), (1000), and (1111).This discrepancy amounts to four out of sixteen possible input combinations. The current architecture is deemed more suitable for operations where the error rate remains below four occurrences.

Table I: Truth Table of Existing Approximate 4:2 Compressor (Architecture 1)

A1	A2	A3	A4	SUM	CARRY
0	0	0	0	0	0
0	0	0	1	1	0
0	0	1	0	1	0
0	0	1	1	1	0
0	1	0	0	0	1
0	1	0	1	0	1
0	1	1	0	0	1
0	1	1	1	1	1
1	0	0	0	0	1
1	0	0	1	0	1
1	0	1	0	0	1
1	0	1	1	1	1
1	1	0	0	0	1
1	1	0	1	1	1
1	1	1	0	1	1
1	1	1	1	1	1

5.2 Existing Approximate 4:2 Compressor (Architecture 2)

The existing architecture 2 for approximate 4:2 compressor is shown in Figure2.

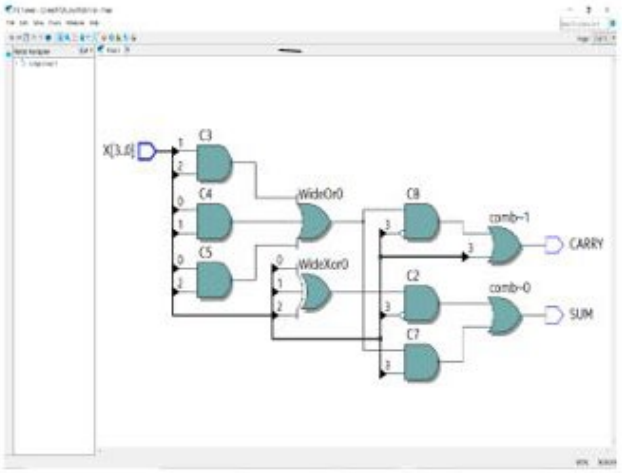

Figure 2: Schematic diagram of existing approximate 4:2 compressor (Architecture 2)

The system employs four inputs labeled as A1, A2, A3, and A4, producing two outputs, CARRY and SUM. The logical expressions governing the generation of CARRY and SUM are as follows:

SUM= (A1⊕A2⊕A3)A4+(A3A2+A2A1+A3A1)A4
CARRY= (A3A2+A2A1+A3A1)A4+A4

Upon analysis of the truth table (Table.2) associated with the existing approximate 4:2 compressor architecture 2, it is evident that erroneous outputs occur for the input configurations (1000) and (1111).The discrepancy amounts to two instances out of a total of sixteen. Consequently, this architecture is deemed more appropriate for applications demanding an error rate of fewer than two occurrences.

Table 2: Truth Table of Existing Approximate 4:2 Compressor (Architecture 2)

A1	A2	A3	A4	SUM	CARRY
0	0	0	0	0	0
0	0	0	1	1	0
0	0	1	0	1	0
0	0	1	1	0	1
0	1	0	0	1	0
0	1	0	1	0	1
0	1	1	0	0	1
0	1	1	1	1	1
1	0	0	0	0	1
1	0	0	1	0	1
1	0	1	0	0	1
1	0	1	1	1	1
1	1	0	0	0	1
1	1	0	1	1	1
1	1	1	0	1	1
1	1	1	1	1	1

6. Proposed Power Efficient Approximate 4:2 Compressor

In this section, we introduce a novel design for an approximate 4:2 compressor. The depicted power-efficient architecture for this compressor is illustrated in Figure 3

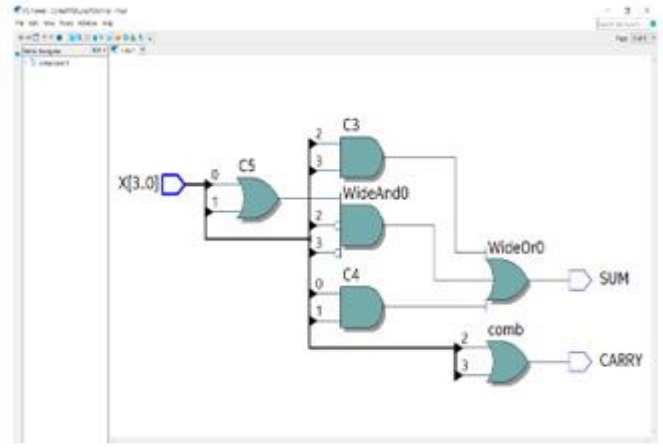

Figure 3: Schematic Diagram of Proposed Approximate 4:2 Compressor

The inputs are labeled as A1, A2, A3, and A4, while the outputs are represented as CARRY and SUM. The logical expressions used to compute CARRY and SUM are detailed below:

SUM= A1A2 + A3A4 + A1A2(A3 + A4)
CARRY= A1 + A2

Upon examination of the truth table (Table.3) for the proposed approximate 4:2 compressor, it is evident that there are discrepancies in the outputs for certain input configurations, specifically for the sequences (0011), (0100), (1000), (1100), and (1111). This discrepancy accounts for five instances out of the total sixteen possible input combinations. Consequently, this design may be deemed more suitable for applications where inaccuracies are required to be below a threshold of five instances.

Table 3: Truth Table of Proposed Approximate 4:2 Compressor

A1	A2	A3	A4	SUM	CARRY
0	0	0	0	0	0
0	0	0	1	1	0
0	0	1	0	1	0
0	0	1	1	1	0
0	1	0	0	0	1
0	1	0	1	0	1
0	1	1	0	0	1
0	1	1	1	1	1
1	0	0	0	0	1
1	0	0	1	0	1
1	0	1	0	0	1
1	0	1	1	1	1
1	1	0	0	1	1
1	1	0	1	1	1
1	1	1	0	1	1
1	1	1	1	1	1

7. Power Analysis

7.1 Existing Approximate 4:2 Compressor (Architecture 1)

The power analysis of the existing 4:2 compressor architecture 1 is given in Fig.4.

Figure 4: Power Analysis of the Existing 4:2 Compressor (Architecture 1)

According to the data presented in Figure 4, the cumulative thermal power dissipation amounts to 729.21mW. This total comprises 3.52mW for core dynamic thermal dissipation, 81.07mW for core static thermal dissipation, and 644.62mW for I/O thermal dissipation.

7.2 Existing Approximate 4:2 Compressor (Architecture 2)

The power analysis of the existing 4:2 compressor architecture 2 is given in Figure 4.

Figure 5: Power Analysis of the Existing 4:2 Compressor (Architecture 2)

According to the data depicted in Figure 5, the overall thermal power dissipation amounts to 729.23mW. This comprises 3.54mW for core dynamic thermal power dissipation, 81.07mW for core static thermal power dissipation, and 644.62mW for I/O thermal power dissipation.

7.3 Modified Approximate 4:2 Compressor

The power analysis of the proposed 4:2 compressor architecture is given in Fig.6.

Figure 6: Power Analysis of the Proposed 4:2 Compressor

From the analysis depicted in Figure 6, it's evident that the overall thermal power dissipation amounts to 729.12mW, comprising 3.43mW for core dynamic thermal dissipation, 81.07mW for core static thermal dissipation, and 644.62mW for I/O thermal dissipation.

8. Conclusion

This study introduces a novel design for approximate 4:2 compressor architectures. The proposed design represents a modification from existing architectures. A comparative evaluation reveals that both Architecture 1 and Architecture 2 exhibit higher power consumption compared to the proposed architecture. While the proposed architecture demonstrates reduced accuracy, as evidenced by the truth table (refer to Table 3), it offers superior power efficiency. Thus, it's apparent that enhancing power efficiency in the approximate 4:2 compressor can be achieved by sacrificing a degree of output accuracy [2].

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References

1. Kong, T., & Li, S. (2021). Design and analysis of approximate 4–2 compressors for high-accuracy multipliers. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 29*(10), 1771-1781.
2. Edavoor, P. J., Raveendran, S., & Rahulkar, A. D. (2020). Approximate multiplier design using novel dual-stage 4: 2 compressors. *IEEE Access, 8*, 48337-48351.